

We claim:

1. A method for programming a one time programmable memory, comprising  
5 the steps of:  
obtaining an array of transistors; and  
programming at least one of said transistors using a hot carrier transistor  
aging technique to alter a characteristic of said at least one of said transistor.
- 10 2. The method of claim 1, wherein said programming step further comprises  
the step of applying a stressful voltage to said at least one of said transistors to cause said  
hot carrier transistor aging.
3. The method of claim 1, wherein said altered characteristic is a change in a  
15 threshold voltage of said at least one of said transistors.
4. The method of claim 3, wherein said programming step further comprising  
the step of applying a stressful voltage to a drain and a gate of said at least one of said  
transistors to cause said change in said threshold voltage of said of said at least one of said  
20 transistors.
5. The method of claim 3, further comprising the step of detecting said  
programmed at least one of said transistors by sensing said change in said threshold  
voltage of said at least one of said transistors.
- 25 6. The method of claim 5, wherein said detecting step further comprises the  
steps of raising a source terminal for each of said array of transistors to a positive  
potential; raising a gate terminal for all transistors along a selected row to a positive  
potential and detecting whether a drain voltage changes from a precharge voltage level to  
30 approximately a cell transistor threshold voltage below said positive gate terminal  
potential.

7. The method of claim 1, wherein said altered characteristic is a change in a saturation current of said at least one of said transistors.
8. The method of claim 7, wherein said programming step further comprising  
5 the step of applying a stressful voltage to a source and a gate of said at least one of said transistors to cause said change in said saturation current of said of said at least one of said transistors.
9. The method of claim 7, further comprising the step of detecting said  
10 programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors.
10. The method of claim 7, wherein said detecting step further comprises the steps of raising the voltage on at least one column in said array of transistors to a positive  
15 potential; raising a gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of voltage decay of at least one column in said array of transistors.
11. A one time programmable memory, comprising  
an array of transistors, wherein at least one of said transistors is  
20 programmed using hot carrier transistor aging to alter a characteristic of said at least one of said transistor; and  
a circuit for sensing said altered characteristic of said at least one of said transistor.
- 25 12. The one time programmable memory of claim 11, wherein said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.
13. The one time programmable memory of claim 11, wherein said altered  
30 characteristic is a change in a threshold voltage of said at least one of said transistors.
14. The one time programmable memory of claim 13, wherein said at least one of said transistors is programmed by applying a stressful voltage to a drain and a gate of

said at least one of said transistors to cause said change in said threshold voltage of said of said at least one of said transistors.

15. The one time programmable memory of claim 13, wherein said circuit  
5 senses said change in said threshold voltage of said at least one of said transistors.

16. The one time programmable memory of claim 15, wherein said circuit  
raises a source terminal for each of said array of transistors to a positive potential; raises a  
gate terminal for all transistors along a selected row to a positive potential and detects  
10 whether a drain voltage changes from a precharge voltage level to approximately a cell  
transistor threshold voltage below said positive gate potential.

17. The one time programmable memory of claim 11, wherein said altered  
characteristic is a change in a saturation current of said at least one of said transistors.

15 18. The one time programmable memory of claim 17, wherein said at least one  
of said transistors is programmed by applying a stressful voltage to a source and a gate of  
said at least one of said transistors to cause said change in said saturation current of said of  
said at least one of said transistors.

20 19. The one time programmable memory of claim 17, wherein said circuit  
senses said change in said saturation current of said at least one of said transistors.

20. The one time programmable memory of claim 17, wherein said circuit  
25 raises a voltage on at least one column in said array of transistors to a positive potential;  
raises a gate terminal of each transistor in a selected row to a positive potential and  
evaluates a rate of voltage decay of at least one column in said array of transistors.

21. A one time programmable memory element, comprising  
30 at least one transistor that is programmed using hot carrier transistor aging  
to alter a transistor characteristic; and  
a circuit for sensing said altered characteristic of said transistor.

22. The one time programmable memory element of claim 21, wherein said altered characteristic is a change in a saturation current of said transistor.

23. The one time programmable memory element of claim 21, wherein said  
5 altered characteristic is a change in a threshold voltage of said transistor.

24. A memory cell, comprising only one transistor, wherein said transistor comprises:

10 a source region;  
a drain region;  
a channel region;  
one silicon-dioxide gate insulator layer; and  
one gate electrode layer.

15 25. The memory cell of claim 24, wherein the memory element is a one time programmable memory element programmed using a hot carrier transistor aging technique to alter a characteristic of said transistor.

26. The memory cell of claim 24, further comprising a plurality of said  
20 memory cells arranged in an array of rows and columns.

27. An integrated circuit, comprising:  
a one time programmable memory, comprising  
an array of transistors, wherein at least one of said transistors is  
25 programmed using hot carrier transistor aging to alter a characteristic of said at least one of said transistor; and  
a circuit for sensing said altered characteristic of said at least one of said transistor.

30 28. The integrated circuit of claim 27, wherein said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

29. The integrated circuit of claim 27, wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors.

30. The integrated circuit of claim 27, wherein said circuit senses said change  
5 in said threshold voltage of said at least one of said transistors.

31. The integrated circuit of claim 27, wherein said altered characteristic is a change in a saturation current of said at least one of said transistors.

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